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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/014,301	12/10/2001	Cong Q. Khieu	004-6390	3139

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EXAMINER	
ANGELO, CAROLINE J	

ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 01/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/014,301	KHIEU ET AL.	
	Examiner	Art Unit	
	Caroline Angelo	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed November 21, 2005 has been entered.

Response to Arguments

2. Applicant's arguments filed November 21, 2005 have been considered but are deemed to be moot in view of the new grounds of rejection necessitated by the applicant's amendment.

3. As to applicant's argument regarding objection to specification (page 10, 2nd paragraph), objection to specification has been withdrawn.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 12, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dow (US 5,306,967) in view of Lin et al. (US 6,414,542 B2).

6. Regarding claim 22, Dow discloses an apparatus of minimizing coupling capacitance between a first signal path and second signal path in an electrical system comprised of:

means for transmitting a first digital signal along the first signal path (figure 1, element 42 and column 4, lines 10-17);

means for transmitting a second digital signal along the second signal path (figure 1, element 41 and column 4, lines 10-17) wherein the second digital signal has a value, "0," opposite a value of the first digital signal, "1," (figure 1, elements 42 and 41 towards the left side of the figure);

means for inverting the value of the first digital signal along the first signal path to match the value of the second digital signal (figure 1, element 52 to the left and column 4, lines 26-31); and

means for re-inverting the first digital signal along the first signal path at a final destination of the first signal path (figure 1, element 52 to the right).

7. However, Dow is silent about storing the second signal in a buffer.

8. In the same field of endeavor, however, Lin discloses an apparatus of minimizing interference comprising means for storing the second digital signal in a buffer along the second signal path (figure 1, element B22, figure 3, element S12 and column 3, lines 37-43).

9. It would have been obvious to one having ordinary skill in the art at the time of the invention to utilize a buffer as taught by Lin in the apparatus of Dow because the buffer of Lin provides propagation time decreases which offset the propagation time increases caused by the inverter, thereby minimizing delays and improving performance.

10. As to claim 1, the steps claimed as method are nothing more than restating the function of the specific components of the apparatus as claimed above and therefore it

would have been anticipated, considering the aforementioned rejection for the apparatus claim 22.

11. As to claim 12, the device claimed is nothing more than restating the specific components of the apparatus as claimed above and therefore it would have been anticipated, considering the aforementioned rejection for the apparatus claim 22.

12. Claims 2-11, 13-21, and 23-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dow in view of Lin and further in view of Tomsio et al. (US 2003/0072332 A1).

13. Regarding claim 23, Dow is silent about time delaying at least one of the first and second digital signals.

14. In the same field of endeavor, however, Tomsio discloses an apparatus of minimizing coupling capacitance interference between a first signal path and a second signal path in an electrical system further comprised of:

means for time delaying at least one of the first and second digital signals (paragraph 33 and figure 2, element 200, a delay circuit receives and delays the signals of the first and second paths).

It would have been obvious to one having ordinary skill in the art at the time of the invention to utilize a delay circuit as taught by Tomsio in the system of Dow because Tomsio minimizes the size of the communication network while reducing the interfering effects of coupling capacitances.

15. Regarding claim 24, Dow discloses an apparatus that meets all limitations of claim 24 except means for inverting the first signal during the storing of the second signal.

16. In the same field of endeavor, however, Lin discloses an apparatus of minimizing interference wherein the means for inverting the first digital signal take place when storing the second digital signal (figure 1, elements B12 and B22, figure 3, element S12 and column 3, lines 40-52).

17. It would have been obvious to one having ordinary skill in the art at the time of the invention to invert the first signal while storing the second as taught by Lin in the apparatus of Dow because Lin reduces the compensation of propagation delay.

18. Regarding claim 25, Dow discloses an apparatus that meets all limitations of claim 25 but Dow is silent about including means for repeating the first and second signals.

19. In the same field of endeavor, however, Lin discloses an apparatus of minimizing interference comprising means for repeating the first digital signal (figure 1, elements B11-B14 and column 6, lines 20-27) and means for repeating the second digital signal (figure 1, elements B21-B24 and column 6, lines 20-27).

20. It would have been obvious to one having ordinary skill in the art at the time of the invention to utilize means for repeating the signals as taught by Lin in the apparatus of Dow because Lin improves the performance and quality of signals received.

21. Regarding claim 26, Dow discloses an apparatus that meets all limitations of claim 26 except repeating the first signal after inversion and repeating the second signal after storing.

22. In the same field of endeavor, however, Lin discloses an apparatus of minimizing interference comprising means for repeating the first digital signal after inverting the first digital signal (figure 1, elements B13-B14 and column 6, lines 20-27), and means for repeating the second digital signal after storing the second digital signal (figure 1, elements B23-B24 and column 6, lines 20-27).

23. It would have been obvious to one having ordinary skill in the art at the time of the invention to repeat the first signal after inversion and repeat the second signal after storing as taught by Lin in the apparatus of Dow because Lin improves the performance of the apparatus.

24. Regarding claim 27, Dow discloses an apparatus that meets all limitations of claim 27, but Dow does not explicitly state that the two signals have the same value for at least one half of the first signal path.

25. In the same field of endeavor, however, Lin discloses an apparatus of minimizing interference wherein the value of the first digital signal and the value of the second digital signal are the same for at least one half of the first signal path (column 4, lines 11-21).

26. It would have been obvious to one having ordinary skill in the art at the time of the invention for the two signals have the same value for at least one half of the first

signal path as taught by Lin in the apparatus of Dow because Lin minimizes the propagation delay.

27. Claims 28-31 recite substantially the same limitations as claim 27 and therefore are similarly analyzed as claim 27 above.

28. As to claims 2-11, the steps claimed as method are nothing more than restating the function of the specific components of the apparatus as claimed above and therefore it would have been obvious, considering the aforementioned rejection for the apparatus claims 23-31.

29. As to claims 13-21, the device claimed is nothing more than restating the specific components of the apparatus as claimed above and therefore it would have been obvious, considering the aforementioned rejection for the apparatus claims 23-31.

Other Prior Art Cited

30. The prior art made of record and not relied upon is considered pertinent to the applicant's disclosure.

31. Saeki et al. (US 4,404,663 discloses an integrated circuit that reduces capacitive interference.

32. Song (US 6,570,931 B1) discloses a transmitter with reduced coupling interference.

33. Ghoshal (US 6,008,705 A) discloses a method of suppressing crosstalk in a transmission system.

34. Zhang (US 5,994,946 A) discloses using staggered inverters to reduce interference from coupling capacitances.

Conclusion

35. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

36. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Caroline Angelo whose telephone number is 571-272-8730. The examiner can normally be reached on 8 am - 4:30 pm Monday through Friday.

38. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

39. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CJA

JAY K. PATEL
SUPERVISORY PATENT EXAMINER